RCC INSTITUTE OF TECHNOLOGY
DIVISION OF YORKVILLE UNIVERSITY, NB

DIG225-06

Latches

Name: _____ **Class: _____**

Objectives

- Design and construct an active low SR Latch
- Design and construct an active high SR Latch
- Design and construct a gated SR Latch
- Design and construct a Contact Bounce Eliminator
- Analyze conditions that could be found in a faulty circuit and apply troubleshooting logic and skills for each of the circuits you build.

Prerequisites

- Digital Design Introduction

Discussion

Latches (and flip-flops) provide one of the basic means of storing one's and zero's. They are used in counters, registers, and memories that are at the very heart of digital electronics. This lab will introduce some of the basic operating characteristics of several types of flip-flops.

Materials Required

- 74LS00 Quad 2 input NAND Gate (1)
- 74LS02 Quad 2 input NOR Gate (1)
- Resistor, 470 ohm (2)

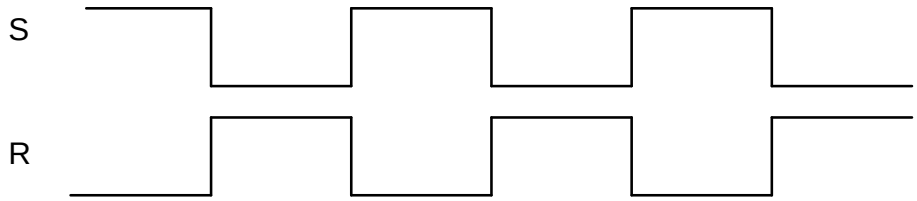
Preparation Questions

1. What is the basic logic function of a latch? _____
2. How many bits of data can a single latch store? _____
3. Name two different types of latches:

   _____ _____
4. Explain the term **bistable**. _____
5. What is the normal output of a SET latch? _____
6. What is the normal output of a RESET latch? _____
7. What is the active input state of a NAND type latch? _____
8. If we apply a low input pulse to both inputs of a NAND type latch, what will be the condition of the latch?

   _____

9. Neatly sketch the waveform for Q and $\overline{Q}$ for a NOR type latch for the inputs shown below. Align the output waveforms properly to the input waveforms.



Q

$\overline{Q}$

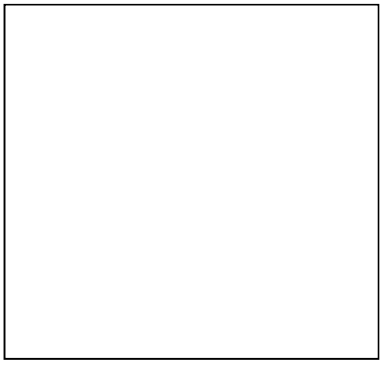
10. Sketch and properly label the **logic symbol** for a latch built using two NAND gates.

11. Sketch the **gate level schematic diagram** for the above latch.

12. Construct your circuit on your breadboard. Use switches for inputs and LEDs for outputs.

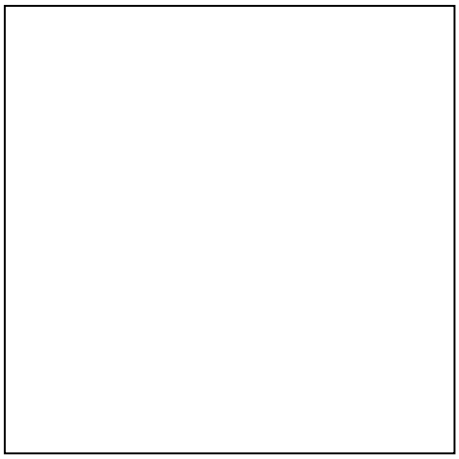
13. Apply power to your circuit. Operate the input switches and complete the truth table at right. In the last column indicate the condition (Set, Reset, Invalid, or Hold.)

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Condition
0	0			
0	1			
1	0			
1	1			



14. Sketch and properly label the **logic symbol** for a latch built using two NOR gates.

15. Sketch the **gate level schematic diagram** for the above latch.

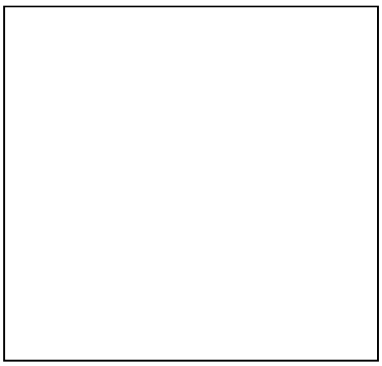


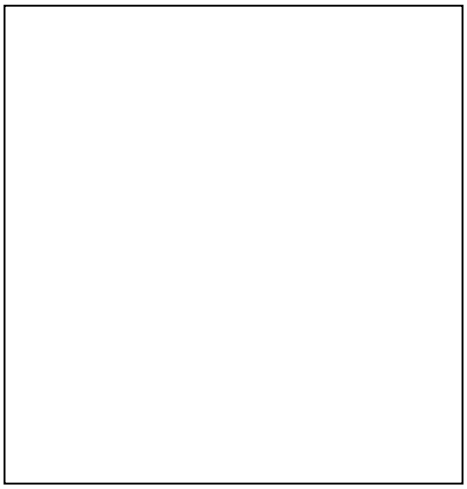
16. Construct your circuit on your breadboard. Use switches for inputs and LEDs for outputs.

17. Apply power to your circuit. Operate the input switches and complete the truth table at right. In the last column indicate the condition (Set, Reset, Invalid, or Hold.)

Inputs		Outputs		
S	R	Q	$\overline{Q}$	Condition
0	0			
0	1			
1	0			
1	1			

18. Sketch and properly label the **logic symbol** for a gated latch built using four NAND gates.





19. Sketch the **gate level schematic diagram** for the above latch.

20. Construct your circuit on your breadboard. Use switches for inputs and LEDs for outputs.

21. Apply power to your circuit. Operate the input switches and complete the truth table at right. In the last column indicate the condition (Set, Reset, Invalid, or Hold.)

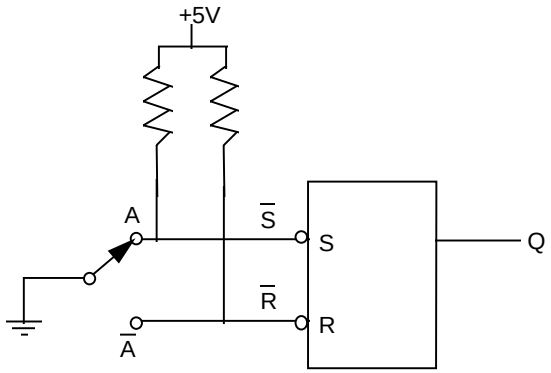
Inputs			**Outputs**		
En	**S**	**R**	**Q**	**$\overline{Q}$**	**Condition**
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Contact Bounce Eliminator

22. Construct the contact bounce eliminator shown below. Use any two equal value pull-up resistors. Use a wire for the switch.

23. Demonstrate your working circuit.

Circuit Demo _____



Input	Output
A	
$\overline{A}$	

24. Complete the truth table for the above circuit.

Insight Questions

25. Compare the input state for the NAND latch in the **Hold** condition to the input state for the NOR latch in the **Hold** condition:

NAND input: _____ NOR input: _____

26. What is the normal output of a latch when it is **SET**? _____

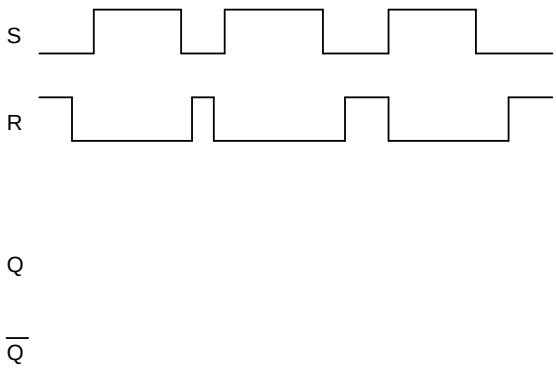
27. If the complementary output of a latch is low, what is the bit value stored? _____

28. If both inputs to a NOR latch are high, then the S input goes low, followed a short time later by the R input going low, what is the value of the bit stored in the latch? _____

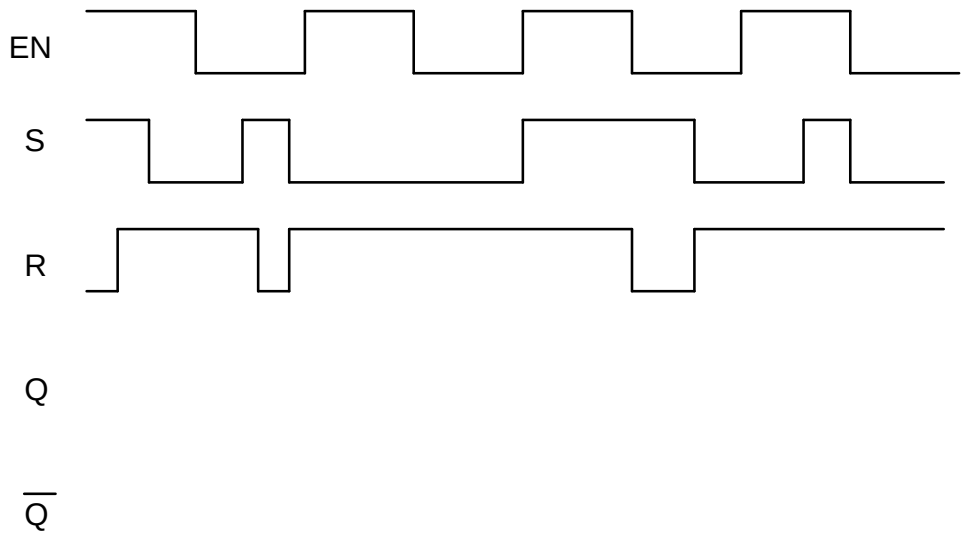
29. If both inputs to a NAND latch are low, then the R input goes high, followed a short time later by the S input going high, what is the value of the state of the latch? _____

30. Is the gated latch you constructed level triggered or edge triggered?_____

31. Sketch the output (Q and $\overline{Q}$) waveforms for a NOR latch with the inputs shown below. Align your state transitions properly.



32. Sketch the output (Q and $\overline{Q}$) waveforms for a Gated NAND latch with the following inputs. Align your state transitions properly.



33. Explain how the Bounce Eliminator circuit removes mechanical bounce from the switch.

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